

Triton-distributed: Programming Overlapping Kernels on Distributed AI Systems with the Triton Compiler

Size Zheng^{1,2,†}, Wenlei Bao^{1,†}, Qi Hou¹, Xuegui Zheng¹, Jin Fang¹, Chenhui Huang¹, Tianqi Li^{1,3}, Haojie Duanmu^{1,4}, Renze Chen^{1,3}, Ruifan Xu^{1,3}, Yifan Guo^{1,5}, Ningxin Zheng¹, Ziheng Jiang¹, Xinyi Di¹, Dongyang Wang¹, Jianxi Ye¹, Haibin Lin¹, Li-Wen Chang¹, Liqiang Lu⁵, Yun Liang³, Jidong Zhai², Xin Liu^{1,†}

¹ByteDance Seed, ²Tsinghua University, ³Peking University, ⁴Shanghai Jiao Tong University, ⁵Zhejiang University

[†]Corresponding authors

Abstract

As the scaling of single chip is gradually approaching its bottleneck, a single accelerator can no longer support the training and inference of existing large language models. Therefore, it has become a pressing need to use distributed system composed of multiple accelerators for training and inference. In a distributed system, there are three fundamental activities occur concurrently: computation, memory access, and communication. In existing training/inference frameworks, these aspects are often optimized independently at different programming levels. As a result, it is difficult for these activities to coordinate with each other and unleash the full performance potential of the cluster.

In this report, we propose Triton-distributed, an extension of existing Triton compiler, to overcome the programming challenges in distributed AI systems. Triton-distributed is the first compiler that supports native overlapping optimizations for distributed AI workloads, providing a good coverage of existing optimizations from different frameworks. First, we integrate communication primitives compliant with the OpenSHMEM standard into the compiler. This enables programmers to utilize these primitives with a higher-level Python programming model. Second, we illustrate how to achieve complex joint optimization of computation, memory access, and communication with the assistance of the compiler. In particular, we show how to use overlapping techniques to hide latency and present our compiler-based programming methods in both single-node and multi-node scenarios. Finally, we showcase the performance of the code generated by our compiler. In a test environment with up to 64 devices, our compiler can fully utilize heterogeneous communication and computation resources to provide effective overlapping and high performance. In many cases, the performance of the generated code can even outperform hand-optimized code. Moreover, the development difficulty and the time cost for development using our compiler are far less than those of low-level programming such as CUDA/C++, which clearly demonstrates significant productivity advantages.

Date: June 13, 2025

Correspondence: Size Zheng at zheng.size@bytedance.com, Wenlei Bao at wenlei.bao@bytedance.com, Xin Liu at liuxin.ai@bytedance.com

Project Page: <https://github.com/ByteDance-Seed/Triton-distributed>

Contents

1	Introduction	3
2	Programming Model	4
2.1	MPMD Programming: Symmetric Memory, Signal Exchange, and Async-Task	4
2.2	Communication Primitives	6
2.3	Example: Inter-node Overlapping AllGather GEMM	6
3	Overlapping Optimizations in Triton-distributed	7
3.1	Optimization Approaches for Overlapping	7
3.2	Intra-node AllGather with Copy Engine	9
3.3	Intra-node ReduceScatter with Copy Engine	9
3.4	Inter-node AllGather with Low-latency Protocol and Multimem Feature	10
3.5	Inter-node ReduceScatter with Heterogeneous Communication	11
3.6	Optimized Communication Kernels on AMD GPUs and more Platforms	13
3.7	Overlapping Computation with Swizzling Optimization	14
3.8	Code Generation Optimization with Auto-Tuning and Resource Partition	16
4	Experiments	17
4.1	Intra-node Kernel Performance on Nvidia GPUs	17
4.2	Inter-node Kernel Performance on Nvidia GPUs	18
4.3	Intra-node Kernel Performance on AMD GPUs	22
5	Conclusion	22

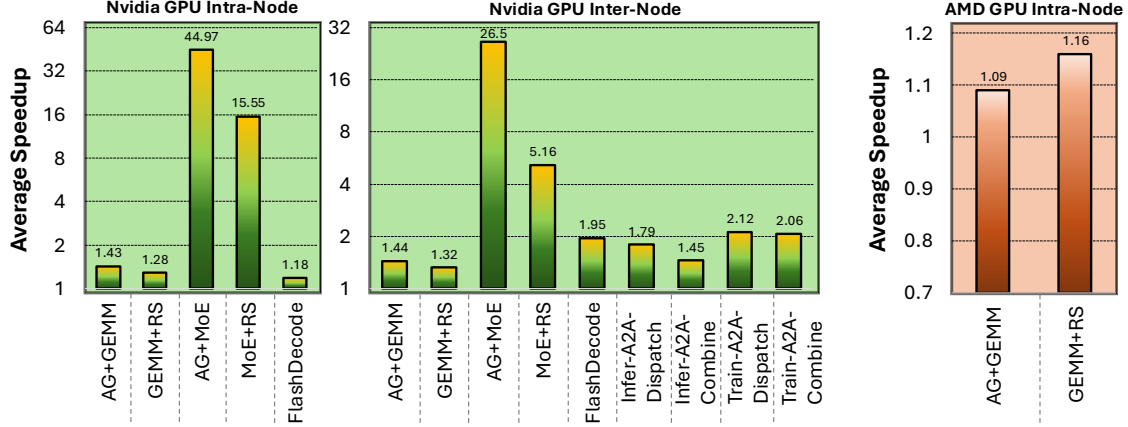


Figure 1 Average Speedup of Triton-distributed to Baselines (PyTorch+NCCL/RCCL).

1 Introduction

With the rapid development of AI, leveraging extremely large language models (e.g., ChatGPT [22], Qwen [30], DeepSeek [7], Doubao [28], etc.), remarkable progress far exceeding expectations has been made in various fields, including chat [22, 28], writing, question answering, coding, mathematics [7, 30], image generation [24], and video generation [23]. The efficient deployment of AI models depends on the co-optimization of underlying hardware and software. At the software level, the main task is to map large-scale computations and parameters onto hardware. As models grow larger, the target hardware for mapping has shifted from single device to multi-accelerator systems.

Distributed programming is notoriously difficult. Despite the extensive work on distributed systems over the past few decades [11, 12, 16–18, 27, 29], these efforts either address only the issues in CPU clusters or require extremely complex engineering optimizations to achieve good performance on AI accelerators. Moreover, there is a significant gap between distributed development and AI algorithm development. Distributed development generally requires programming in CUDA/C++, while algorithm development is often carried out in Python. This inherently necessitates cross-language programming. As a result, most users are proficient in optimizing only one of these two aspects. To achieve both algorithm development and underlying optimization simultaneously, one needs to bridge a significant programming gap. It usually also requires cross-team collaboration, which further leads to a decrease in development efficiency.

Over the past decades, the development of high-performance operators using Python programming has emerged as a key research area, attracting extensive exploration from both academia and industry. This process led to the emergence of numerous compilers [5, 9, 10, 13–15, 26, 32, 37–39], but after years of validation, the outstanding compilers that have withstood the test of time [15, 31, 32] still mainly focus on single-device scenarios. In terms of single chip code generation capability, these compilers have already matched the level of experts. For instance, on NVIDIA GPUs, their performance rivals that of CUTLASS [20] and cuBLAS [19]. Some compilers, such as Triton [32], have been adapted by numerous manufacturers to support a wide range of AI chips [2, 25]. However, with the advent of LLMs, research on compiler optimization for single chip has almost converged (although hardware advancements continue to drive the development of new compilation techniques). Overall, compiler research has entered a distributed era. Early studies on distributed compilers, such as distributed Halide [8] and DISTAL [33], were confined to non-large-model scenarios and fell short of meeting the distributed requirements of emerging LLMs. Additionally, previous distributed compilers were inclined to propose proprietary DSLs rather than align with Python.

For LLMs, the key requirement for distributed optimization becomes computation-communication overlapping. Previously, in small-scale distributed training/inference, communication overhead wasn’t a critical cost issue. However as cluster number scales exponentially, overlapping computation with communication becomes vital. For example, ByteDance’s COMET [35] recently saved millions of GPU hours through this technique,

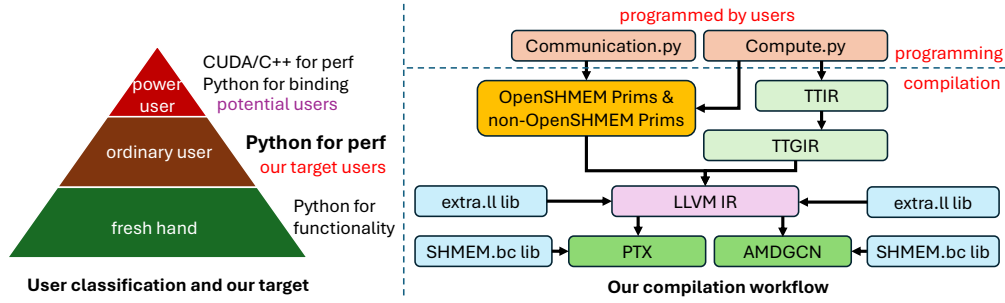


Figure 2 Overview of our compilation stack.

equivalent to millions of dollars in cost savings. The ability to overlap computation with communication has exceeded the scope of existing compilers, leaving this optimization accessible only to a few teams with exceptional engineering capabilities [3, 4, 36].

In this report, we propose Triton-distributed, an distributed compiler extension based on open-source Triton. Triton-distributed supports native fine-grained computation-communication overlapping using compiler-assisted primitives. Both computation implementation and communication optimization are fully achieved at the Python level, yielding performance comparable to or better than CUDA/C++ implementations. In Figure 1, we show the overall speedup of Triton-distributed to NCCL/RCCL on Nvidia GPUs and AMD GPUs for a wide range of workloads. The speedup ranges from $1.09\times$ to $44.97\times$. Triton-distributed supports both overlapping tasks such as AllGather GEMM (AG+GEMM) and GEMM ReduceScatter (GEMM+RS) as well as communication-only tasks such as expert-parallel AllToAll (inference low-latency AllToAll dispatch/combine and training high-bandwidth AllToAll dispatch/combine). All these workloads are implemented using our compiler-assisted primitives. Our compiler translates these primitives into NVSHMEM/ROCSHMEM implementations during compilation, enabling communication across both single-node and multi-node GPU clusters. Notably, implementing these workloads requires minimal modifications to Triton’s original compute code: developers only focus on adding communication logic.

In Figure 2, we present an overview of our compilation stack. Users can program communication and computation parts separately in Python. The communication part is implemented with OpenSHMEM primitives, which are further lowered to LLVM IR along with a bitcode library. The computation part goes through the original Triton compilation stack to LLVM IR. Finally, PTX or AMDGCN are generated and executed on target accelerators. Our compiler is mainly designed for ordinary users who are familiar with Python-level LLM model development and have an average knowledge of performance optimization. Power users who are experts in low-level programming may also use our compiler to reduce development overhead without much performance degradation. Furthermore, leveraging Triton’s multi-hardware support, our solution also works on AMD GPUs and other NPUs. Based on our compiler, we have also built a higher-level compiler TileLink [40] with higher-level communication primitives (which are not included in this report).

2 Programming Model

To use our compiler, we first introduce the programming model. Then we introduce the primitives supported by our compiler. Finally, we show an AllGather GEMM example written using our programming model.

2.1 MPMD Programming: Symmetric Memory, Signal Exchange, and Async-Task

Our programming model follows the MPMD (multiple programs multiple data) model. The MPMD model allows communication and computation tasks to run in parallel and cooperate with each other to complete a global task. The core of our programming model includes three concepts: symmetric memory, signal exchange, and async-task.

Symmetric Memory: Each rank allocates a memory buffer in the global scope with the same size. Each memory buffer has a separate address space, and there is no uniform virtual address (UVA) space from a

Table 1 Our Communication Primitives

Primitive	Explanation
OpenSHMEM Primitives	
<i>my_pe</i>	Get the current device id
<i>n_pes</i>	The number of devices in the world
<i>int_p</i>	Put an integer to remote device
<i>remote_ptr</i>	Convert local shared memory pointer to remote pointer
<i>barrier_all</i>	Barrier all the devices
<i>sync_all</i>	Synchronize all the devices
<i>quiet</i>	Ensure completion of shared memory operation of calling device
<i>fence</i>	Ensure order of shared memory operation of calling device
<i>getmem</i>	Blocking get data from remote device
<i>getmem_nbi</i>	Non-blocking get data from remote device
<i>putmem</i>	Blocking put data to remote device
<i>putmem_nbi</i>	Non-blocking put data to remote device
<i>putmem_signal</i>	Blocking put data and write signal to remote device
<i>putmem_signal_nbi</i>	Non-blocking put data and write signal to remote device
<i>signal_op</i>	Perform signal set/add operation to remote
<i>signal_wait_until</i>	Wait local signal until condition is meet
<i>broadcast</i>	Broadcast data into all the other ranks
non-OpenSHMEM Primitives	
<i>wait</i>	Locally wait a signal until it equals to some given value
<i>consume_token</i>	used with <i>wait</i> primitive to create data dependency
<i>notify</i>	Notify a remote signal, similar to <i>signal_op</i> primitive
<i>atomic_cas</i>	Atomic compare and swap
<i>atomic_add</i>	Atomic add value
<i>ld_acquire</i>	Load with acquire semantic
<i>red_release</i>	Reduction add with release semantic
<i>multimem_ld_reduce</i>	Multimem load data and perform reduction
<i>multimem_st</i>	Multimem broadcast data

global perspective. Remote memory buffers cannot be accessed directly via pointers. To perform remote data transfer, specific primitives are required.

Signal Exchange: Operations on each rank use signals to communicate with each other in a consistent manner. A signal is a data object that resides in symmetric memory. There is a fixed set of operations to manipulate signals, including setting the value of a signal, increasing the value of a signal, checking the value of a signal, and performing a spin-lock on a given signal.

Async-Task: Operations such as data transfer and computation are treated as asynchronous tasks that run in parallel. Async-tasks can be synchronized through signals. Note that even on the same rank, the operations are asynchronous. For different hardware backends, there are different ways to implement async-tasks. For GPUs, multi-streaming and multi-threading are common choices. Multi-streaming relies on runtime task queues to launch different tasks simultaneously, while multi-threading leverages parallel hardware units.

For the example in Figure 3, we visually demonstrate the three core concepts. In this example, we use 2 nodes, each with 2 ranks. The left part of Figure 3 shows the symmetric memory buffers of each rank and the signal exchange between different tasks within the same rank or across ranks. In the right part, we use a timeline to show that at each rank, three tasks run in parallel: inter-node P2P (point-to-point) data transfer, intra-node P2P data transfer, and computation. Tasks at different ranks also run in parallel. Each rank launches the three tasks simultaneously. The computation task is a single kernel that runs on the device; the order of the

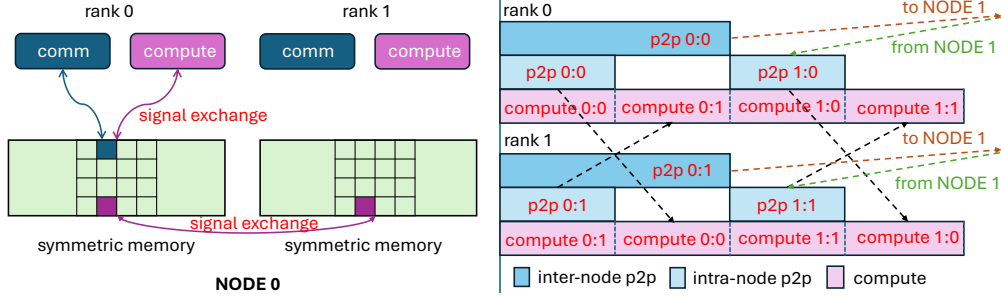


Figure 3 Explanation of Symmetric Memory, Signal Exchange, and Async-Task.

tiles of the computation kernel is carefully tuned so that the computation never waits for the communication (note that the computation order at rank 0 and rank 1 is different). In this example, we use $0:0$ to denote the data tile from node 0, rank 0. Other notations are similar.

2.2 Communication Primitives

For a distributed system, the essence of designing primitives is to model communication patterns effectively. The design of communication primitives depends on the system’s architecture, such as the interconnection topology and bandwidth. Currently, mainstream distributed systems like Nvidia GPUs and AMD GPUs support the OpenSHMEM standard and have implemented their own shared-memory communication primitive libraries. Although other NPU accelerators do not currently support the OpenSHMEM standard, it can be expected that this standard will be widely adopted in the future. Therefore, the new primitives we added to the compiler should also align with the OpenSHMEM standard.

Currently, we provide two sets of primitives: OpenSHMEM primitives and non-OpenSHMEM primitives. We list these two sets of primitives in Table 1. For OpenSHMEM primitives, their corresponding implementations can be found in NVSHMEM and ROC SHMEM for Nvidia and AMD GPUs respectively. Non-OpenSHMEM primitives (e.g. *wait*, *consume_token*, and *notify*) provide complementary functions. These primitives are specially designed for optimization purposes. For example, *wait* is used with *consume_token* to construct data dependency between signal operations, and the following MMA operations for better compiler-based pipelining. Load/store primitives with specific semantics are used for low-latency communication or signal exchange within a node. These primitives include atomic operations, load with acquire semantics, store with release semantics, and load/store with multitem semantics.

2.3 Example: Inter-node Overlapping AllGather GEMM

In Figure 4 we show how to program an inter-node overlapping AllGather GEMM using our compiler. The AllGather GEMM program is composed of three parts: the communication part, the computation part, and the host side. For the communication part (on the left), we assign different tasks to different threadblocks. Part of the threadblocks are responsible for intra-node dispatch, while the other threadblocks perform inter-node data transfer. These two groups of threadblocks run in parallel to overlap inter-node data transfer and intra-node data transfer. For the computation part (up-right), we just reuse Triton’s original GEMM implementation and add only two primitives in the GEMM kernel. The first primitive *wait* produces a token related to a signal, while the second primitive *consume_token* consumes the token and creates data dependency between the token and the following data load. Different tiles in the GEMM kernel runs in parallel, each tile waits for its own signal, overlapping its dependent communication and other tiles’ computation. Finally, the host-side code (bottom-right) allocates symmetric memory and launches the communication part and the computation part on different streams. The communication part and the computation part both requires SMs (streaming multiprocessors) for execution. The execution timeline of this AllGather GEMM is demonstrated in Figure 3.

```

@triton.jit
def producer_allgather(
    A, signal, num_elem_per_rank,
    rank, local_world_size, world_size):
    pid = tl.program_id(0)
    node = rank // local_world_size
    local_rank = rank % local_world_size
    n_nodes = world_size // local_world_size
    if pid < local_world_size - 1:
        peer = ((local_rank + pid + 1) % local_world_size
                + node * local_world_size)
        for i in range(n_nodes):
            seg = (local_rank +
                  ((node + i) % n_nodes) * local_world_size)
            if tid(0) == 0:
                signal_wait_until(signal + seg, EQ, 1)
                __syncthreads() # wait for remote node's send
            putmem_signal(
                A + seg * num_elem_per_rank, # wait for
                A + seg * num_elem_per_rank, # possible
                signal + seg, # previous
                1, SET, peer) # intra-node send # producer, if no
                                # producer,
                                # default set to 1
        else:
            pid = pid - local_world_size + 1
            if tid(0) == 0:
                signal_wait_until(signal + rank, EQ, 1)
                __syncthreads()
            peer = (local_rank + (node + pid + 1) % n_nodes
                  * local_world_size)
            putmem_signal(
                A + rank * num_elem_per_rank,
                A + rank * num_elem_per_rank,
                signal + rank,
                1, SET, peer) # inter-node send
    # AllGather Part

```

```

@triton.jit
def consumer_gemm(A, B, C, signal):
    pid = tl.program_id(0)
    pid_m, pid_n = ... # calculate pids
    offs_A, offs_B, offs_C = ... # calculate offsets for A, B, C
    acc = tl.zeros([TILE_M, TILE_N])
    for k in range(K//TILE_K):
        token = wait( # wait and consume pair
            signal + pid_m, 1, "gpu", "acquire", waitValue=1)
        a_ptrs = consume_token(A + offs_A, token)
        a_data = tl.load(a_ptrs)
        b_data = tl.load(b_ptrs)
        tl.dot(a_data, b_data, acc)
        offs_A, offs_B = ... # update offsets for A and B
    tl.store(C + offs_C, acc)
    # GEMM Part

```

```

def ag_gemm(A, B, C, signal)
    # omit preparing values such as num_elem_per_rank
    with comm_stream():
        grid = (local_world_size + n_nodes - 2, 1, 1)
        producer_allgather[grid](
            A, signal, num_elem_per_rank,
            rank, local_world_size, world_size)
        with compute_stream():
            grid = ((M//TILE_M) * (N//TILE_N), 1, 1)
            consumer_gemm[grid](A, B, C, signal)
    # Host Side

```

```

A = create_tensor([global_M, K])
signal = create_tensor([world_size])
    # Allocate symmetric memory

```

Figure 4 Code Example of AllGather GEMM for Inter-node

3 Overlapping Optimizations in Triton-distributed

Using Triton-distributed, we can cover common overlapping optimizations for distributed workloads. In this section, we first summarize common overlapping optimizations. Then, we show kernel implementations using our compiler. To demonstrate the generality of our compiler, we show the kernel optimizations on two platforms: Nvidia GPUs and AMD GPUs. For kernel implementation, we show the one-sided equivalent of collective communication and how to optimize them for different purposes (high-bandwidth or low-latency). The term one-sided means that all communication operations are programmed from the perspective of a single rank, which is different from collective communication programming, where communication is programmed against all ranks. After this, we show how to overlap the communication kernels with computation kernels using signals. To achieve the best performance, tile swizzling is required. Tile swizzling changes the order of communication and computation, making it possible to achieve the maximum overlap in distributed systems. Finally, we explain our performance tuning techniques, including automatic distributed program tuning and manual analytical configurations.

3.1 Optimization Approaches for Overlapping

Our Triton-distributed supports a wide range of optimization techniques. Although these optimizations are proposed or implemented originally in previous frameworks, Triton-distributed is the first to cover all

Table 2 Optimization Approaches and Comparison with Other Frameworks

Name	NCCL	PyTorch	TE	Pallas	CoCoNet	FLUX	DeepEP	Ours
Intra-Node Swizzle	■	✓	✓	■	✓	✓	■	✓
Inter-Node Swizzle	■	✗	✗	■	✓	✓	■	✓
Inter-NUMA Swizzle	■	✗	✗	✗	✗	✗	■	✓
Copy Engine	✓	✓	✓	✓	✓	✓	✗	✓
High-BW Link	✓	✓	✓	✓	✓	✓	✓	✓
Network Comm.	✓	✓	✗	✓	✓	✓	✓	✓
PCIe Comm.	✓	✓	✗	✗	✗	✓	✗	✓
OpenSHMEM Support	✗	✗	✗	✗	✗	✓	✓	✓
Low-latency Protocol	✓	✗	✗	✗	✗	✓	✗	✓
Multimem Feature	■	✗	✗	✗	✗	✗	✗	✓
Fusion	✗	✗	✗	■	✓	✓	✓	✓
Code Generation	✗	✗	✗	✓	✓	✗	✗	✓
Nvidia/AMD	✓/✗	✓/✓	✓/✗	■/✗	✓/✗	✓/✗	✓/✗	✓/✓

these optimizations within one framework. We list 13 different optimizations that are required for different optimization purposes.

- **Intra-Node Swizzle:** Swizzle is to change the order of communication operations and computation operations so that they can better overlap with other. Intra-node swizzle is to perform swizzling within a node.
- **Inter-Node Swizzle:** Inter-node swizzle is to perform swizzling across different nodes.
- **Inter-NUMA Swizzle:** For multi-socket systems, cross-NUMA communication performance is hard to optimize because of NUMA effect. Swizzling across different NUMAs could improve overlapping performance.
- **Copy Engine:** GPUs and NPUs employ dedicated memory copy units to perform communication. Using these units for communication is also important for overlapping within single node.
- **High-BW Link:** Utilizing high-bandwidth links such as NVLink and xGMI is critical for both intra-node and inter-node communication. Both copy engine and computing cores (e.g., SMs) can map communication operations to high-bandwidth links.
- **Network Communication:** Cross-node communication relies on network communication. Network communication optimization refers to map communication operations to network devices and schedule them to overlap with other operations.
- **PCIe Communication:** For accelerators that only support PCIe communication (e.g., L20), we need to schedule communications among PCIe links to avoid resource contention.
- **OpenSHMEM Support:** This optimization refers to using OpenSHMEM implementations (NVSHMEM or ROC SHMEM) to schedule communication operations.
- **Low-latency Protocol:** This optimization is to use low-latency protocol (proposed in NCCL) to achieve barrier-free communication.
- **Multimem Feature:** This optimization utilize hardware features to perform broadcast/reduction through dedicated instructions.
- **Fusion:** This optimization refers to fusing processing logics into communication, such as data casting, transposing, simple arithmetic operations, etc.

- **Code Generation:** This optimization refers to the ability to generate code just-in-time and to support tuning to further improve performance.
- **Nvidia/AMD:** This is used to represent hardware-specific optimizations. For Nvidia GPUs, optimizations include warpgroup MMA instructions, warp specialization, TMA instructions, etc. For AMD GPUs, optimizations include persistent kernel optimization and software pipelining.

In Table 2 we show the comparison of Triton-distributed to previous representative distributed overlapping frameworks. We use green check-mark (✓) to show that the framework supports the corresponding optimization; use yellow square (■) to represent the corresponding optimization is potentially applicable in the framework, but not for sure; use red cross (✗) to represent that the optimization is not supported yet. Triton-distributed supported all the listed optimizations.

On NVIDIA H800 GPU clusters, we focus on three collective communication types: AllGather, ReduceScatter, and AllToAll. These three types are well supported in communication libraries such as NCCL [21]. However, these libraries perform synchronization before and after collective communication. As a result, overlapping is only available at the operator level (e.g., stream control and asynchronous wait). To achieve fine-grained overlapping, we need to break these collective communication operations into one-sided point-to-point communication operations and synchronize these operations with other computation operations through signals.

3.2 Intra-node AllGather with Copy Engine

For intra-node AllGather, we use copy engine for data transfer. Copy engine is a dedicated DMA (direct memory access) engine in GPU for data transfer between devices. Copy engine can be triggered using runtime interfaces such as *CudaMemcpy* or *CudaMemcpyAsync*. For one-sided communication, depending on the direction of data transfer, there are two implementation variants: push mode and pull mode. Using push mode, we can omit one synchronization operation but the data arrival order cannot be controlled; while using pull mode, we need an additional synchronization but the data arrival order can be controlled.

In Algorithm 1, we show the pseudo-code for push mode AllGather. $remote_ptr(T, r)$ is used to get symmetric remote buffer pointer of T at rank r , which is then used to create a remote buffer through $make_buffer$.

Algorithm 1 One-sided Push-mode Intra-node AllGather

```

1: Input: Symmetric Buffer  $T$ , Signal  $S$ , Local Buffer  $L$ 
2: for  $r$  in range(WORLD_SIZE) do
3:    $remote\_buf = make\_buffer(remote\_ptr(T, r) + RANK \times L.size())$ 
4:    $remote\_buf.copy\_ (L, L.size())$  // Memory Copy
5:    $remote\_sig = remote\_ptr(S, r) + RANK$ 
6:    $set\_signal(remote\_sig)$  // Notify the consumer
7: end for
```

In Algorithm 2 we show pull mode one-sided AllGather. Compared to push mode, pull mode needs to perform local copy at first (line 3) and then uses a *barrier_all* to make the result of local copy visible to all the other ranks. Then, other ranks are able to copy the data to their own buffer.

3.3 Intra-node ReduceScatter with Copy Engine

ReduceScatter is the reverse operation of AllGather. ReduceScatter can also be implemented in push or pull mode. We only show push mode in Algorithm 3. The one-sided ReduceScatter is composed of two parallel parts. For the first part, local data shard is pushed to all the other ranks after the producer generates one tile of data; for the second part, local reduction is done and produces the final output. The two parts communicate with each other through signals.

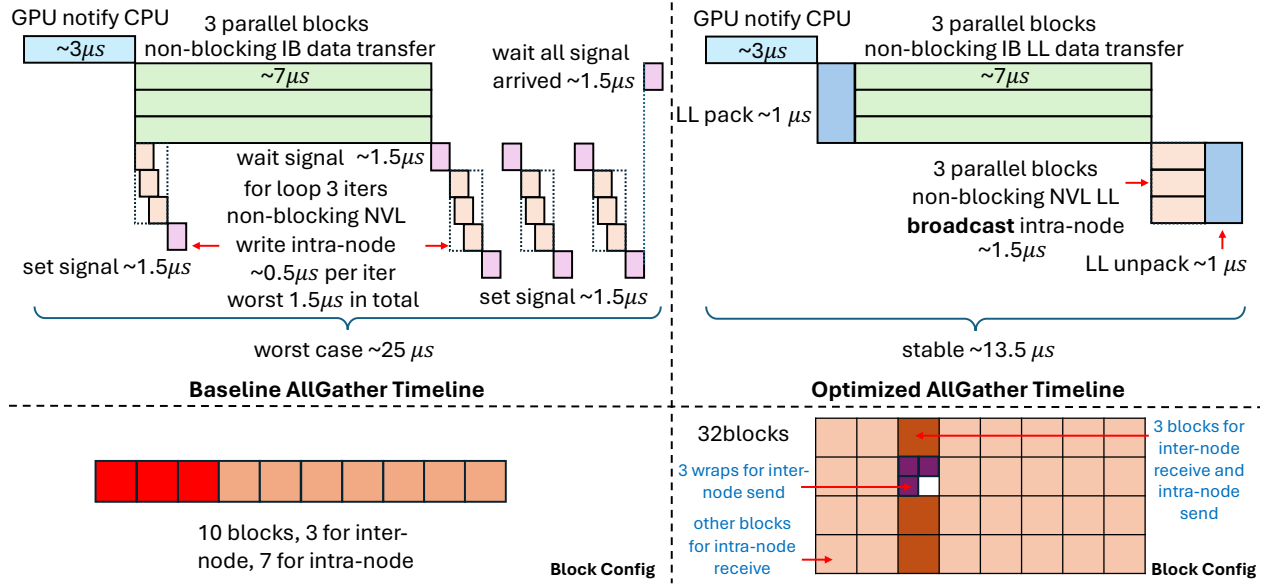


Figure 5 The Timeline of Baseline AllGather and Low-latency AllGather.

Algorithm 2 One-sided Pull-mode Intra-node AllGather

```

1: Input: Symmetric Buffer  $T$ , Signal  $S$ , Local Buffer  $L$ 
2:  $\text{local\_t\_buf} = \text{make\_buffer}(T + \text{RANK} \times L.\text{size}())$ 
3:  $\text{local\_t\_buf.copy\_}(L, L.\text{size}())$ 
4:  $\text{set\_signal}(S + \text{RANK})$ 
5:  $\text{barrier\_all}()$  // Make the local copy visible to all the other ranks
6: for  $r$  in  $\text{range}(\text{WORLD\_SIZE})$  do
7:   if  $r$  is not  $\text{RANK}$  then
8:      $\text{remote\_buf} = \text{make\_buffer}(\text{remote\_ptr}(T, r) + r \times L.\text{size}())$ 
9:      $\text{local\_t\_buf} = \text{make\_buffer}(T + r \times L.\text{size}())$ 
10:     $\text{local\_t\_buf.copy\_}(\text{remote\_buf}, L.\text{size}())$ 
11:     $\text{set\_signal}(S + r)$ 
12:   end if
13: end for

```

3.4 Inter-node AllGather with Low-latency Protocol and Multimem Feature

Inter-node AllGather requires overlapping the inter-node data transfer and the intra-node data transfer. For the code example in Figure 4, we have shown how to achieve such overlapping through assigning asyc-tasks to different threadblocks. However, this version of AllGather is only designed for high-bandwidth, not for low-latency. For inference scenarios, low-latency AllGather is required for efficient parallel execution. The message size in AllGather is small, so processing delay and queuing delay are not critical. The main overhead of communication comes from propagation delay.

The AllGather implementation in Figure 4 relies on loops to do data transfer, as a result, the data transfer operations are not launched at the same time. As shown on the left half of Figure 5, using such an implementation, during the execution of AllGather, there is some skew among the data transmission operations sent to different ranks. Since the amount of transmitted data is very small, in the worst-case, the result of the skew is similar to sending data one by one, which leads to an extended overall delay. For example, the transmission via NVLink takes approximately $0.5 \mu\text{s}$, but after the skew, it may take up to $1.5 \mu\text{s}$ to transmit the data from the other 3 nodes at worst. In addition, each P2P data transfer requires a pair of signal operations (set signal and wait signal), causing additional overhead.

To address these issues and achieve low-latency AllGather, we propose to use non-OpenSHMEM primitives to achieve intra-node broadcast and use low-latency protocol (LL) for inter-node data transfer. In detail, we use *multimem_st* primitive to do NVLink broadcast. The multimem instruction in Nvidia PTX instruction set is used to store the same data to all the other ranks within one node, which costs about $1.5\mu s$. For inter-node communication, we use LL protocol, which relies on a hardware feature of Nvidia GPU that 8 bytes data store/load is atomic across ranks. Other low-latency protocol such as LL128 (which relies on the hardware feature of NVLink) can also be leveraged. Considering that we are targeting small message scenarios, LL works perfect. To implement LL protocol, we store data and flags together into an 8 bytes data chunk and send the data directly to remote ranks, while the remote receivers use a spin-lock to check if the flag is the same as expectation to tell if the data has arrived. LL protocol is fast but doubles the message size (due to flags in message), which is suitable for small message scenarios but not for large message size.

In Algorithm 4, we show the pseudo-code of our low-latency AllGather. We use *BLOCK_ID* to denote the current threadblock index, use *LOCAL_WORLD_SIZE* to denote the number of ranks in one node, use *LOCAL_RANK* to denote the rank index of the current device, use *NODE_ID* to denote the node index that the current device belongs to, use *N_NODES* to denote the number of nodes in total, and use *WORLD_SIZE* to denote the number of ranks from all the nodes in total. We use *recv_LL_pack* to perform LL receive operation without decoupling data from flags, while *recv_LL_unpack* performs LL receive operation and separates the data from the flags. In Algorithm 4, we need totally *WORLD_SIZE* threadblocks and the block role configuration is shown in Figure 5. One of the threadblock is responsible for inter-node data send and local data receive (line 11-18), three threadblocks are responsible for inter-node data receive and intra-node data send (line 6-9), while the other blocks are responsible for intra-rank receive (line 21-22).

The timeline of the low-latency AllGather is shown in the right part of Figure 5. The estimated latency is $13.5\mu s$, which is better than the estimated latency of the baseline implementation (about $25\mu s$).

Algorithm 3 One-sided Push-mode Intra-node ReduceScatter

```

1: Input: Symmetric Buffer  $T$ , Signal from producer  $P$ , Signal for Reduction  $S$ , Local Buffer  $L$ , Reduce
   Output buffer  $R$ 
2: // In Stream 1
3: for  $r$  in range( $WORLD\_SIZE$ ) do
4:   wait_signal( $P + RANK$ ) // Wait for the producer to generate one tile of data
5:   remote_buf = make_buffer(remote_ptr( $T, r$ ) +  $RANK \times R.size()$ )
6:   remote_buf.copy_( $L + RANK \times R.size(), R.size()$ )
7:   remote_sig = remote_ptr( $S, r$ ) +  $RANK$ 
8:   set_signal(remote_sig)
9: end for
10: // In Stream 2
11: for  $r$  in range( $WORLD\_SIZE$ ) do
12:   wait_signal( $S + r$ )
13:   tiled_buf = make_buffer( $T + r \times R.size()$ )
14:    $R = R + tiled\_buf$ 
15: end for

```

3.5 Inter-node ReduceScatter with Heterogeneous Communication

The inter-node ReduceScatter can be decomposed into three stages: namely intra-node scatter, local reduction, and inter-node P2P communication. Since the local reduction operation requires SM resources, we aim to maximize bandwidth while minimizing resource usage to ensure that the computation (e.g., GEMM) performance is affected as little as possible.

in Algorithm 5, we show the pseudo-code of our inter-node ReduceScatter. We use *P2P_send* to denote inter-node P2P communication. To optimize resource usage and enhance communication efficiency, we employ an overlapping strategy for intra-node and inter-node communications. We schedule the intra-node scatter on one stream, while the local reduction and P2P communication are assigned to another stream. The scatter

Algorithm 4 One-sided Low-latency Cross-Node AllGather

```
1: Input: Symmetric Buffer  $T$ , Low-latency Buffer  $L$ , Signal  $P$ , Bytes per Rank  $bytes$ 
2:  $peer\_node\_id = BLOCK\_ID / LOCAL\_WORLD\_SIZE$ 
3:  $peer\_local\_rank = BLOCK\_ID \% LOCAL\_WORLD\_SIZE$ 
4: if  $peer\_local\_rank == LOCAL\_RANK$  then
5:   if  $NODE\_ID != peer\_node\_id$  then
6:      $seg = peer\_node\_id \times LOCAL\_WORLD\_SIZE + LOCAL\_RANK$ 
7:      $recv\_LL\_pack(L + seg \times bytes \times 2, L + seg \times bytes \times 2)$ 
8:      $multimem\_st(L + seg \times bytes \times 2, L + seg \times bytes \times 2)$ 
9:      $recv\_LL\_unpack(T + seg \times bytes, L + seg \times bytes \times 2)$ 
10:   else
11:      $LL\_pack(L + RANK \times bytes \times 2, T + RANK \times bytes)$ 
12:      $\_\_syncthreads()$ 
13:     if  $WARP\_ID < N\_NODES$  and  $WARP\_ID != NODE\_ID$  then
14:        $peer = WARP\_ID \times LOCAL\_WORLD\_SIZE + LOCAL\_RANK$ 
15:        $putmem\_nbi\_warp(L + RANK \times bytes \times 2, L + RANK \times bytes \times 2, peer)$ 
16:     end if
17:      $seg = peer\_node\_id \times LOCAL\_WORLD\_SIZE + LOCAL\_RANK$ 
18:      $multimem\_st(L + seg \times bytes \times 2, L + seg \times bytes \times 2)$ 
19:   end if
20: else
21:    $seg = peer\_node\_id \times LOCAL\_WORLD\_SIZE + peer\_local\_rank$ 
22:    $recv\_LL\_unpack(T + seg \times bytes, L + seg \times bytes \times 2)$ 
23: end if
```

Algorithm 5 One-sided Push-mode Cross-node ReduceScatter

```
1: Input: Local Buffer  $L[M, N]$ , Signal from producer  $P$ , Signal for inter node communication  $S$ , Reduce
   Output buffer  $R$ 
2: Input:  $partial\_rs\_buf = \text{Symmetric Buffer}(N\_NODES, M\_PER\_RANK, N)$ 
3: Input:  $scatter\_buf = \text{Symmetric Buffer}(LOCAL\_WORLD\_SIZE, M\_PER\_RANK, N)$ 
4:  $M\_PER\_RANK = M / WORLD\_SIZE$ 
5:  $M\_PER\_NODE = M / N\_NODES$ 
6: for  $n$  in  $\text{range}(N\_NODES)$  do
7:   // In Stream 0: intra node scatter
8:   for  $r$  in  $\text{range}(LOCAL\_WORLD\_SIZE)$  do
9:      $gr = r + NODE\_ID * LOCAL\_WORLD\_SIZE$ 
10:     $\text{wait\_signal}(P + gr)$ 
11:     $\text{remote\_buf} = \text{make\_buffer}(\text{remote\_ptr}(\text{scatter\_buf}[LOCAL\_RANK], gr))$ 
12:     $\text{remote\_buf.copy\_}(L + gr \times M\_PER\_RANK \times N, M\_PER\_RANK \times N)$ 
13:   end for
14:    $\text{barrier\_all\_intra\_node}(\text{stream0})$ 
15:   // In Stream 1: local reduction and inter node P2P
16:    $\text{stream1.wait}(\text{stream0})$ 
17:    $rs\_cur\_node = \text{Reduce}(\text{scatter\_buf}, \text{dim}=0)$ 
18:    $\text{target\_rank} = LOCAL\_RANK + n \times LOCAL\_WORLD\_SIZE$ 
19:    $P2P\_send(rs\_cur\_node, \text{remote\_ptr}(partial\_rs\_buf[NODE\_ID], \text{target\_rank}))$ 
20: end for
21:  $\text{barrier\_all}()$ 
22:  $R = \text{Reduce}(partial\_rs\_buf, \text{dim}=0)$ 
```

operation is completed by the copy engine and does not require SM; P2P communication only requires 1 SM, and the number of SMs for local reduction is the minimum required value calculated based on hardware specifications.

Taking 8×H800 as an example (around 170 GB/s NVLink maximum bandwidth), each GPU is connected to a CX7 InfiniBand 400 Gb/s RDMA network card (around 45 GB/s maximum bandwidth), the communication volume is $B = \frac{M_{PER_RANK} \times N \times sizeof(dtype)}{10^9}$ GB. The time for P2P communication is $\frac{B}{45}$, and the time for scatter is $\frac{(8-1) \times B}{170}$. So the left time for reduction is $\frac{(8-1) \times B}{170} - \frac{B}{45}$. It can be inferred that if the bandwidth of the local reduction operator exceeds 470 GB/s, perfect overlap can be achieved. Therefore, on H800 GPU, it is sufficient to assign only a small number of SMs (no more than 15) for local reduction.

3.6 Optimized Communication Kernels on AMD GPUs and more Platforms

On AMD MI308X GPU cluster, we focus on AllGather and ReduceScatter collective communications. Similarly, RCCL [1] is the typical communication library used on AMD GPUs to perform these collective operations, and often coupled with synchronizations before and after execution. Thus the overlapping is limited within scope of operator-level. We employ similar signal-based approach to synchronize computation and communication to achieve fine-grained overlapping.

Intra-node AllGather with Copy Engine

For intra-node AllGather on AMD, we still utilize copy engine for data transfer between different GPUs. Runtime APIs such as *hipMemcpyAsync* is used to control copy engine on AMD GPU, and options like *hipMemcpyDeviceToDeviceNoCU* can be used to specify not use GPU compute units (CU) to avoid affecting computations happen at the same time.

Unlike Nvidia H800 cluster that GPU connected through NVLink system, on AMD MI308X cluster each GPU connects with others via bidirectional link. Therefore, to maximize the bandwidth, the data transfer needs to be launched on multiple streams simultaneously. After the data transfer, corresponding signals need to be set to notify the consumers. Typically these can be achieved using driver APIs such as *cuStreamWriteValue* or *hipStreamWriteValue* on Nvidia and AMD GPUs respectively. However, these driver APIs seem to interfere with computation kernels and cause considerable delay on AMD GPUs. Thus we have to use other approach to workaround, here we launched another data transfer solely for signals.

Besides the push or pull mode variants for one-sided communication, communication tile size also plays an important factor in optimization. In AllGather, communication tiling is decoupled from computation tiling to avoid any interference. Tuning communication tiling independently allows us to find a best trade off between overlapping opportunity and communication efficiency, minimizing effective communication time. Moreover the communication tile order also matters, it needs to align with corresponding consumer computation to minimizing overall delay. In other words, it requires the computation tile coordinate swizzling to align with the arriving order of the communication tile.

Intra-node ReduceScatter with Fusion

For ReduceScatter, due to the previous mentioned interfere issue, we fused scatter part with producer kernel to store the output data directly to other ranks once the tile of data gets ready and avoid the need for any driver API. Then the reduction part is performed follow by *barrier_all* and produce the final output.

Here the producer kernel has to be modified to decouple the tile size with communication tile, and add the communication tile size as another tuning factor in autotune. Again the tile coordinate swizzling needs to align with communication tile order to utilize all the bidirectional links so as to maximize the bandwidth.

Optimizations on More Platforms Although we only show optimized kernels for GPUs currently, we can support other platforms similarly. To achieve this, we require the target hardware to support the three core concepts in our programming model. First, the hardware should support symmetric memory allocation and access, which is expected to conform to the OpenSHMEM standard. Second, the hardware should support signal exchange, including signal setting, increasing, checking, and spin-locks. Third, the hardware should support async-tasks, allowing us to map specialized tasks spatially to different hardware units. With the support of

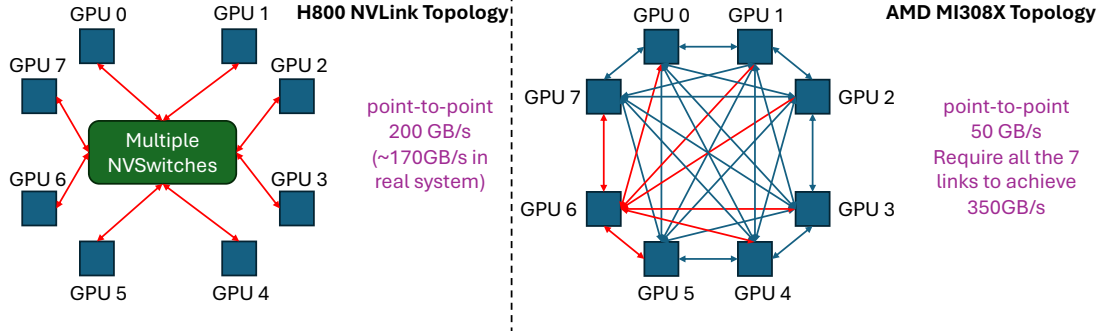


Figure 6 Topology of Nvidia GPUs and AMD GPUs

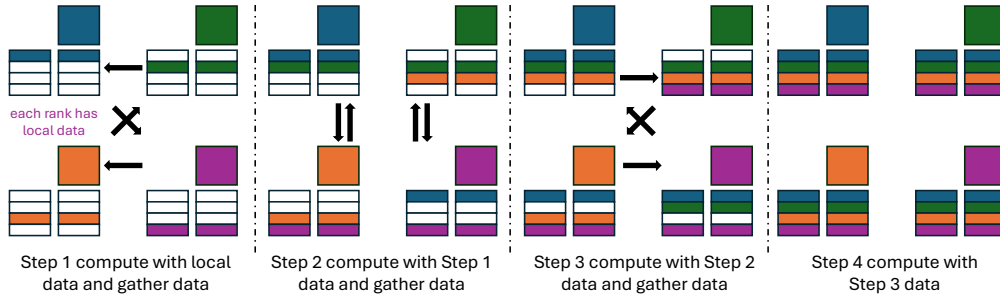


Figure 7 Swizzle Example for Intra-node AllGather GEMM on Nvidia GPUs. (Assume 4 ranks.)

the three core concepts, we can port our OpenSHMEM and non-OpenSHMEM primitives to the hardware platform accordingly.

3.7 Overlapping Computation with Swizzling Optimization

So far, we have mainly discussed collective communication parts of optimized overlapping kernels. In this section, we introduce the optimizations for overlapping the computation part. Efficient GPU kernels, either Nvidia or AMD GPU, both rely on tiling to exploit parallelism and locality. And there is a tile mapping logic, from a thread block index to a tile coordinate. By controlling the order of tiles, we can both improve cache utilization (e.g., L2 cache) and communication efficiency (by reducing the critical path). The optimization that controls the order of tiles is called swizzling.

The design of tile swizzle requires the tile swizzle order in computation kernels align with the communication tiles for two purposes: 1) avoid potential memory contention and 2) minimize tile data transfer time [3]. Moreover, because of the complexity of topology connections between GPUs in one node or multi-nodes, as well as different vendors, tile swizzling in computation kernels has to consider all these variants that reflects in collective communication to maximize overlapping and minimize overall latency.

For Nvidia GPUs and AMD GPUs, they use different topology for interconnection. In Figure 6, we show the difference between them. Nvidia H800 GPUs use NVSwitches to connect the 8 GPUs within one node. Each pair of GPUs can communicate with each other with a maximum of 200 GB/s uni-direction bandwidth. But AMD MI308X GPUs use a full-mesh topology, where each GPU connects to the other 7 GPUs with 7 different links. Each link has a maximum of 50 GB/s uni-direction bandwidth. The aggregated bandwidth for a single GPU is 350 GB/s.

Different operators require different swizzle methods to fully utilize the interconnection bandwidth. Without loss of generality, we show the swizzle methods for AllGather GEMM and GEMM ReduceScatter. The swizzle methods for other operators can be designed similarly. For AllGather GEMM on Nvidia GPUs, we show the swizzle in Figure 7. We use a small number of ranks (4 ranks) for simplicity. At the beginning of AllGather GEMM, each rank occupies a chunk of data (local data). For the first step, each rank uses its own local

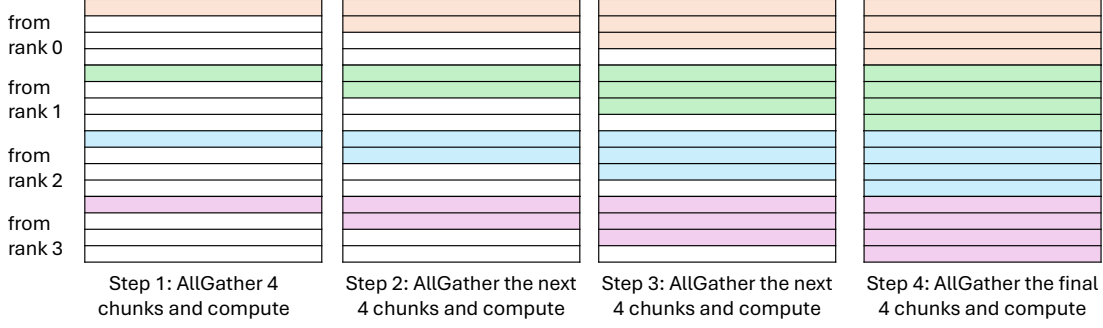


Figure 8 Swizzle Example for Intra-node AllGather GEMM on AMD GPUs. (Assume 4 ranks.)

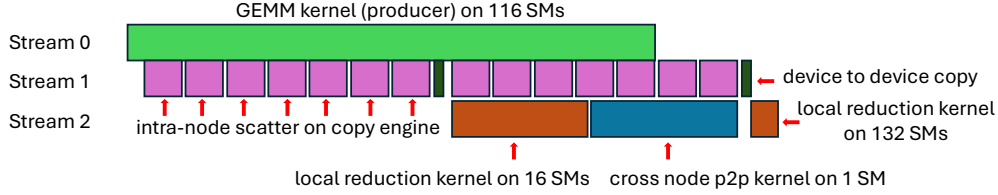


Figure 9 The Timeline of Inter-node GEMM ReduceScatter.

data to compute part of outputs, and at the same time, each rank P2P gathers the next chunk data from another rank. So the GEMM kernel of each rank starts from a unique tile index, which is relevant to its own rank index. For the second step, each rank uses the data gathered from the previous step to compute part of outputs, and meanwhile, P2P gathers the next chunk of data from another rank. As the bandwidth of each link of NVLink can reach the peak bandwidth, each rank only gathers data from one another rank at a time.

For AllGather GEMM on AMD GPUs, the swizzle design is different. If we only gather the next chunk of data from another one GPU at a time, the maximal available bandwidth is only 50 GB/s. To fully utilize the bandwidth, each rank should gather data chunks from all the other ranks at each step. In Figure 8 we show the sizzle method for AMD GPUs. For each chunk of data in each rank, we further tile them into sub-chunks. For each step, each rank gathers all the next sub-chunks from all the other ranks. Figure 8 shows the swizzle view from a single rank. For Step 1, it gathers the first sub-chunk from all the other ranks and complete the GEMM computation using these sub-chunks. For the second step, it gathers the next set of sub-chunks. The remaining steps follow a similar pattern.

Besides the design for intra-node topology, we also provide swizzling design for inter-node overlapping. We use GEMM ReduceScatter for illustration as this example is the most representative one. For simplicity, we use 2 nodes with totally 8 ranks (4 ranks per node). The swizzling steps are shown in Figure 10. We decompose the GEMM ReduceScatter into three stages as explained previously. For intra-node scatter stage, each rank performs 7 remote data transfers and one local data copy (for its own rank index). The intra-scatter stage is repeated 2 times for each rank. To overlap the most of communication, we should arrange the local copy step of intra-node scatter to the tailing position of the stage. So each rank starts its own computation from the next chunk of data relative to its rank index, rather than from its own rank index. Similarly, to overlap inter-node P2P data transfer, each node should start its computation from the data chunks needed by the other node. As a result, the Step 1 in Figure 10 uses a shift for the starting position for each tile of computation and each chunk of data. In detail, rank 0 starts its GEMM for the data required by rank 5, rank 1 starts computation for rank 6, and so forth. After each step of computation, each rank sends its partial sum to the next rank within the same node for local reduction. After all the ranks within one node get all the chunks of data, each rank P2P sends the partial sum to the peer rank in another node (Step 5). After this, all the ranks within the same node repeat the Steps 2-4 to produce the final output.

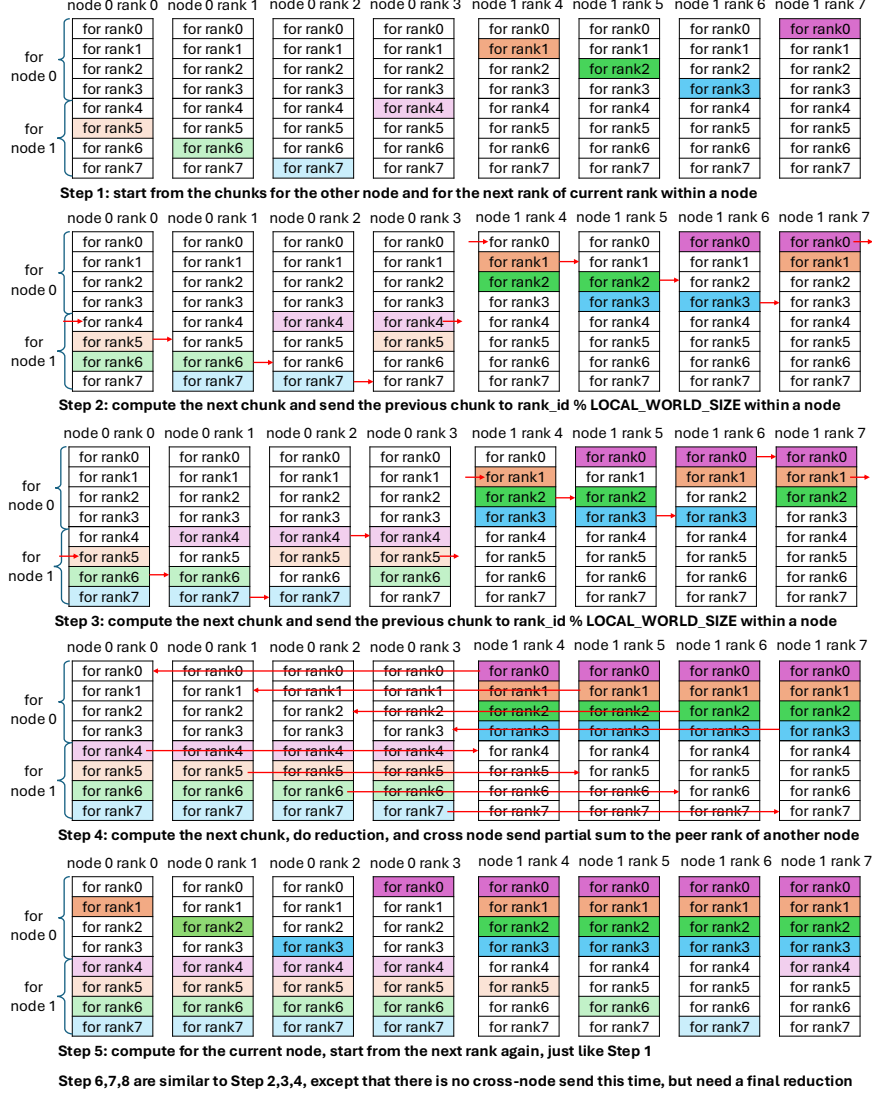


Figure 10 Swizzle Example for Inter-node GEMM ReduceScatter. (Assume 2 nodes, each with 4 ranks.)

3.8 Code Generation Optimization with Auto-Tuning and Resource Partition

Besides swizzling optimization, we also leverage two important optimizations for better performance. The first is tiling factor tuning, and the second is resource partition.

For tiling factor tuning, we develop an autotuner tailored for distributed kernels. The autotuners used in previous compilers [5, 32] iteratively launch a single kernel with different tiling configurations on a single device to discover the best one. However, unlike tuning on a single device, distributed kernel tuning involves the communication and synchronization between different kernels across multiple devices. This requires us to consider both the synchronization needs of the kernel launch itself and the synchronization of the tuning results. For example, since we focus on overlapping kernels, we need to reset all the signals every time we profile the generated code, and we cannot just repeatedly execute the target kernel like the previous autotuner, as this would disrupt the synchronization conditions. To this end, our autotuner can accept a target function that wraps the overlapping kernels (encompassing communication, computation, and host-side launch logic), including the kernels requiring tuning. The target function is executed iteratively as a whole. In each iteration, the kernel that needs tuning within the target function is executed only once. The profiling and enumeration

Table 3 List of Our Optimized Kernels

Name	Explanation	Tested Hardware Cluster
AG+GEMM-intra	Intra-node AllGather GEMM Overlapping	8 H800 and MI308X GPUs.
GEMM+RS-intra	Intra-node GEMM ReduceScatter Overlapping	8 H800 and MI308X GPUs.
AG+MoE-intra	Intra-node AllGather MoE GroupGEMM Overlapping	8 H800 GPUs
MoE+RS-intra	Intra-node MoE GroupGEMM ReduceScatter Overlapping	8 H800 GPUs
FlashDecode+AG-intra	Intra-node Flash Decode AllGather and Combine	8 H800 GPUs
AllToAll-intra	Intra-node Low-latency AllToAll	8 H800 GPUs
AG+GEMM-inter	Inter-node AllGather GEMM Overlapping	16 H800 GPUs
GEMM+RS-inter	Inter-node GEMM ReduceScatter Overlapping	16 H800 GPUs
AG+MoE-inter	Inter-node AllGather MoE GroupGEMM Overlapping	16 H800 GPUs
MoE+RS-inter	Inter-node MoE GroupGEMM ReduceScatter	16 H800 GPUs
FlashDecode+AG-inter	Inter-node Flash Decode AllGather and Combine	16 and 32 H800 GPUs
AllToAll-inter	Inter-node Low-latency AllToAll	16, 32, and 64 H800 GPUs

of tuning configurations are progressively carried out as the target function iterates. Finally, upon completion of a kernel’s tuning, a global synchronization is performed to aggregate the tuning information from different devices, thereby selecting a globally unified best configuration.

Resource partition is to spatially map the computation and communication to different processing units (e.g. SMs). For intra-node overlapping kernels, the communication can be mapped to copy engine, and the computation can fully utilize all the compute cores (SMs or CUs). For inter-node overlapping kernels, communication also requires computing cores to complete remote memory access. And the insight in resource partition is to make sure all the async-tasks can overlap with each other and complete at the same time (i.e. avoid long tails). Take inter-node GEMM ReduceScatter introduced previously as example, the timeline of our overlapping kernels is shown in Figure 9, on H800 GPUs, the GEMM kernel uses 116 SMs, the intra-node scatter is mapped to copy engine, the cross node P2P kernel uses 1 SM, the first local reduction kernel uses 16 SMs, and the second local reduction kernel uses 132 SMs. With this configuration, perfect overlapping can be achieved.

4 Experiments

In this section, we demonstrate the performance of our optimized kernels. We list the supported kernels in Table 3. We use both Nvidia H800 GPUs and AMD MI308X GPUs to test the performance. The scale of our cluster ranges from 8 GPUs to 64 GPUs. For each case, we list the problem shapes and baseline accordingly.

4.1 Intra-node Kernel Performance on Nvidia GPUs

AllGather GEMM

For AG+GEMM-intra, we compare with PyTorch+NCCL (PyTorch uses cuBLAS [19] for GEMM) and FLUX [3] (FLUX uses CUTLASS [20] for GEMM). For GEMM performance, Triton’s generated code can achieve roughly 95% the performance of cuBLAS and CUTLASS. Although our GEMM performance is not the best, we still achieve better AG+GEMM performance due to enhanced overlapping. On average, we achieve $1.42\times$ speedup to PyTorch+NCCL and $1.09\times$ speedup to FLUX.

GEMM ReduceScatter

For GEMM+RS-intra, we also compare to PyTorch+NCCL and FLUX. Our overlapping design is different from FLUX. FLUX fuses the scatter operation into GEMM kernel and performs a global synchronization before local reduction. We use a separate stream to perform scatter asynchronously and perform local reduction on another stream. Overall, we achieve $1.28\times$ speedup to PyTorch+NCCL and $1.30\times$ speedup to FLUX.

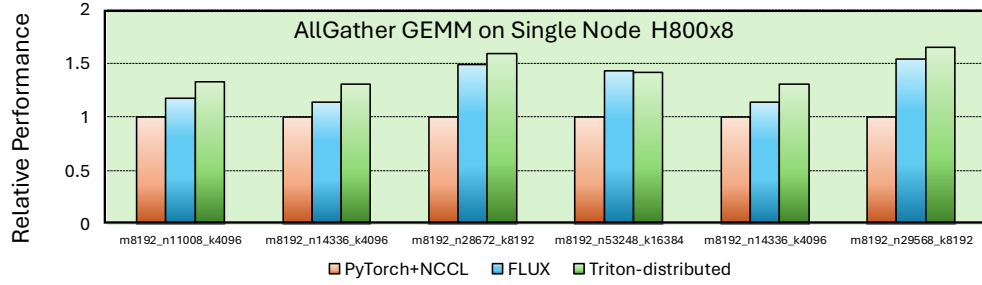


Figure 11 Performance of Intra-node AllGather GEMM on 8 H800 GPUs.

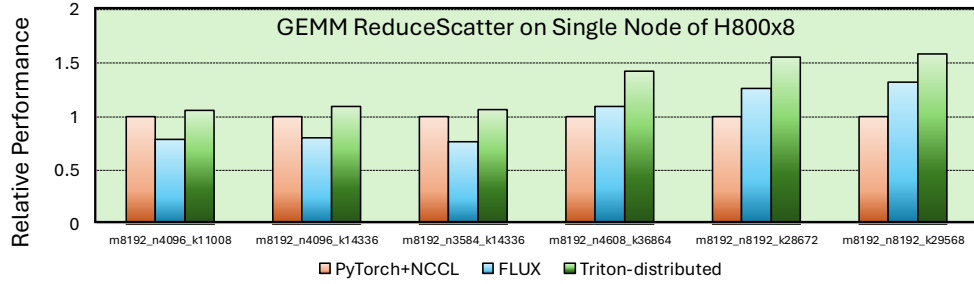


Figure 12 Performance of Intra-node GEMM ReduceScatter on 8 H800 GPUs.

AllGather MoE

For AG+MoE-intra, FLUX fused MoE kernels focus on expert parallel (EP), while we use tensor parallel (TP). The other baseline PyTorch+NCCL implementation uses Python loops for GroupGEMMs, which is a weak baseline. As a result, our performance is much better compared to this baseline. Overall, the average speedup to PyTorch+NCCL is 44.97 \times . We show the test shapes and our performance in absolute values in Table 4.

MoE ReduceScatter

For MoE+RS-intra, the overlapping kernels include MoE GroupGEMM, topk reduction, and reduce scatter. Similar to AG-MoE-intra, we show our own performance in absolute values. The performance of the PyTorch+NCCL baseline is much worse to compare. We achieve on average 15.55 \times speedup. The test shapes and performance results are shown in Table 5.

4.2 Inter-node Kernel Performance on Nvidia GPUs

To scale the overlapping kernels to more nodes, we employ the optimizations introduced in previous sections and show the performance results of different kernels.

AllGather GEMM

For AG+GEMM-inter, we test the performance on 2 nodes of H800 GPUs. We mainly compare our performance with PyTorch+NCCL, and FLUX using metrics reported in its original paper with some problem size data not available. The results are shown in Figure 13. We exceed PyTorch+NCCL consistently, with an average speedup of 1.33 \times and achieve 95.60% the performance of FLUX.

GEMM ReduceScatter

For GEMM+RS-inter, we also use 2 nodes of H800 GPUs for test. We use FLUX’s performance reported in the original paper as baseline. We also compare to PyTorch+NCCL. The results are shown in Figure 14. Overall, we can achieve 96.36% the performance of FLUX. Compared to PyTorch+NCCL, the average speedup is 1.42 \times .

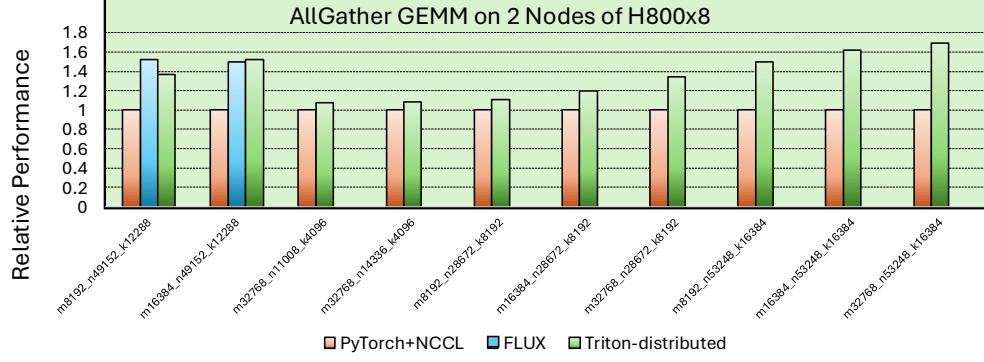


Figure 13 Performance of Inter-node AllGather GEMM on 16 H800 GPUs.

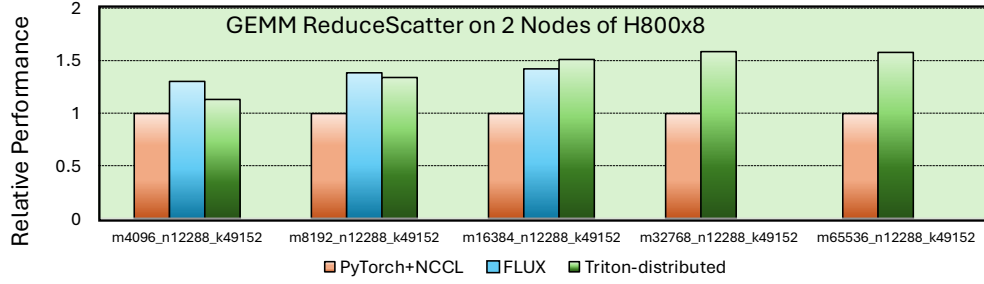


Figure 14 Performance of Inter-node GEMM ReduceScatter on 16 H800 GPUs.

AllGather MoE and MoE ReduceScatter

By reusing the inter-node AllGather and ReduceScatter kernels, we also scale MoE kernels to 2 nodes. For AG+MoE-inter, we list the performance in absolute values in Table 4. The results show that scaling AG+MoE kernel from 1 node to 2 nodes increases the latency almost linearly, demonstrating good weak scaling. However, for MoE+RS-inter, the scaling is not good. As shown in Table 5, when scaling the MoE+RS from 1 node to 2 nodes, the latency increase is not linear. This indicates that a dedicated ReduceScatter kernel is required for MoE+RS to achieve better performance, which is left for future. Overall, compared to PyTorch+NCCL, the average speedup of AG+MoE-inter is $26.50\times$, the average speedup of MoE+RS-inter is $5.16\times$.

Distributed Flash Decoding

Previous work [6, 34] only implements flash decoding kernel for a single device. We scale flash decoding to more devices, both intra-node and inter-node. Flash decoding is a bandwidth bound kernel, so the main evaluation metric is the achieved HBM bandwidth for each GPU. The peak HBM bandwidth for H800 GPU

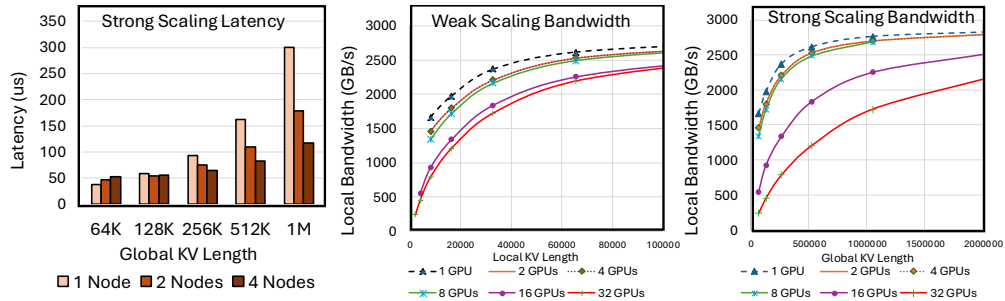


Figure 15 Performance of Distributed Flash Decoding.

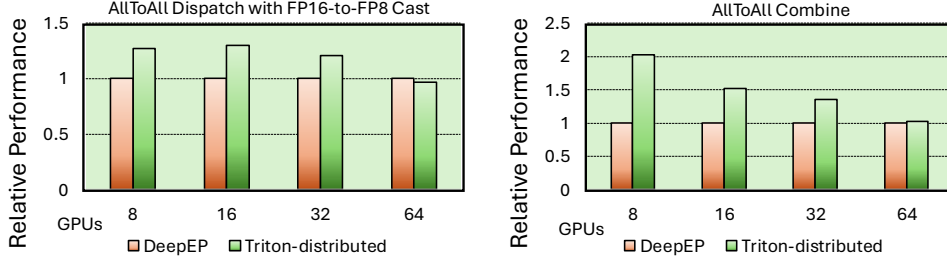


Figure 16 Performance of AllToAll.

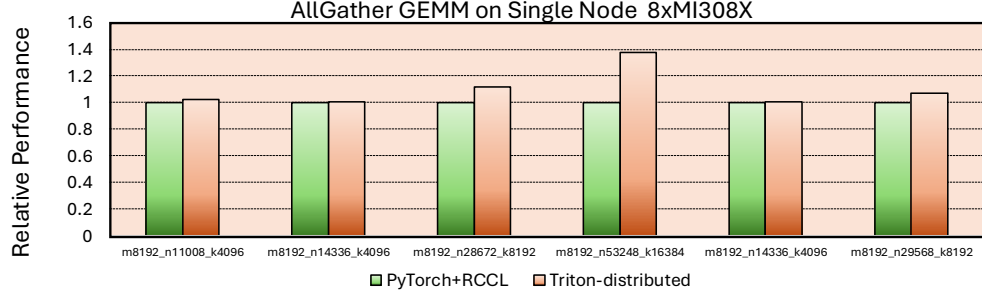


Figure 17 Performance of Intra-node AllGather GEMM on AMD GPUs.

is around 3 TB/s. By gradually increasing the number of GPUs involved in our distributed flash decoding, we can observe the bandwidth change of each GPU. We use batch size 1 to show the performance of flash decoding. As shown in Figure 15, when increasing the number of GPUs, if we keep the KV cache length of each GPU unchanged (weak scaling), the achieved HBM bandwidth remains high even for 32 GPUs (1.7 TB/s for 32K KV cache length per GPU). If we keep the global KV cache length unchanged (strong scaling), the achieved HBM bandwidth decreases as the number of GPUs increases. The decoding latency indicates that for global KV cache length less than 256K, increasing the number of GPUs is not beneficial. For very long KV cache lengths (e.g. 1M), the more GPUs used, the lower latency can be achieved. The good scalability of our distributed flash decoding comes from the low-latency AllGather kernel. This distributed flash decoding paves the way to the efficient execution of extremely long context decoding, which might be useful for future reasoning models that are more powerful than existing models.

Low-latency AllGather

Besides NVLink, we also support PCIe communication. To show the performance on PCIe clusters, we use L20 GPUs. L20 only supports PCIe communication. We implement low-latency AllGather for PCIe and test the performance on 8 L20 GPUs and 16 L20 GPUs (2 nodes). The results are shown in Figure 19. We compare to

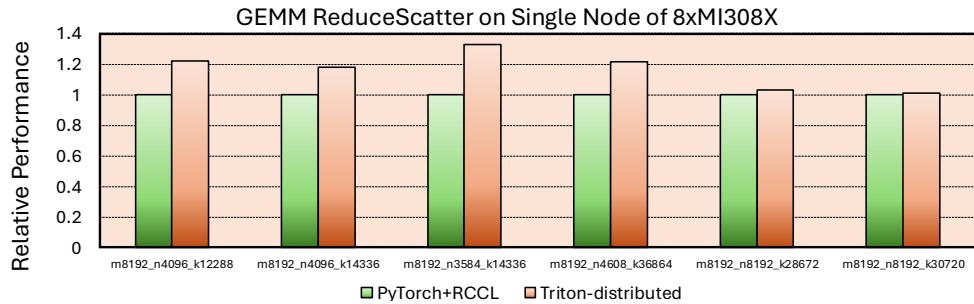


Figure 18 Performance of Intra-node GEMM ReduceScatter on AMD GPUs.

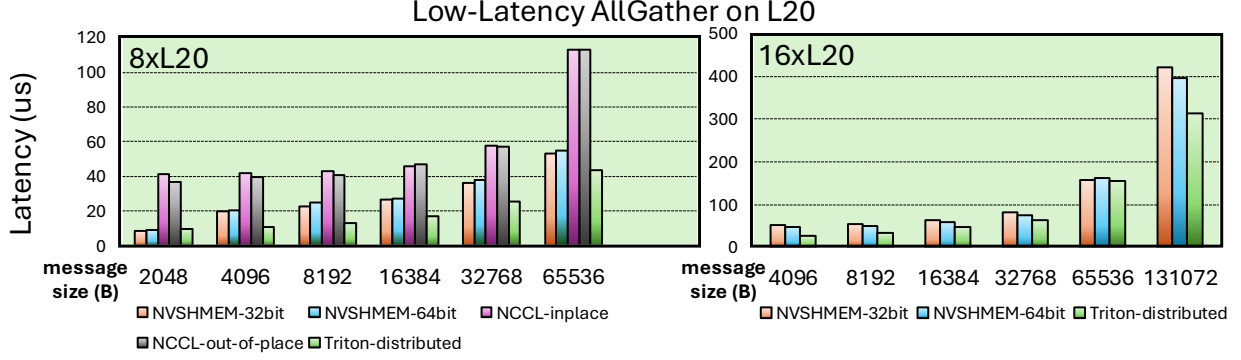


Figure 19 Performance of Low-latency AllGather on L20 GPUs.

Table 4 Test Shapes for AllGather MoE and Performance (ms).

Name	tokens/rank	in hidden	out hidden	experts	topk	Ours		PyTorch	
						Intra	Inter	Intra	Inter
AG+MoE-1	256	2048	1408	60	4	0.33	0.45	23.95	28.84
AG+MoE-2	512	2048	1408	60	4	0.40	1.37	26.25	29.77
AG+MoE-3	1024	2048	1408	60	4	0.58	1.80	30.42	43.31
AG+MoE-4	2048	2048	1408	60	4	0.97	3.07	55.63	63.73
AG+MoE-5	256	14336	4096	8	2	0.54	1.01	7.05	19.92
AG+MoE-6	512	14336	4096	8	2	0.72	1.89	26.34	36.07
AG+MoE-7	1024	14336	4096	8	2	1.19	3.41	52.99	67.61
AG+MoE-8	2048	14336	4096	8	2	2.10	6.51	107.32	129.30
AG+MoE-9	256	16384	6144	8	2	0.81	1.39	11.02	27.29
AG+MoE-10	512	16384	6144	8	2	1.06	2.21	39.65	52.32
AG+MoE-11	1024	16384	6144	8	2	1.66	4.32	80.46	101.61
AG+MoE-12	2048	16384	6144	8	2	2.92	8.28	159.69	192.67
AG+MoE-13	512	1408	2048	64	6	0.45	0.84	29.25	38.17
AG+MoE-14	1024	1408	2048	64	6	0.67	1.26	48.86	56.77
AG+MoE-15	2048	1408	2048	64	6	1.18	2.18	74.26	90.44

NVSHMEM builtin AllGather (fcollect) and NCCL builtin AllGather. NVSHMEM-32bit refers to using 32bit data type for communication, while NVSHMEM-64bit refers to using 64bit data type for communication. NCCL-inplace and NCCL-out-of-place are different AllGather implementations in NCCL. NCCL-inplace uses the input buffer as output buffer, while NCCL-out-of-place uses another output buffer. For single node, we achieve the lowest latency on average, achieving bandwidth improvement compared to NVSHMEM ($1.40\times$ to 32bit and $1.48\times$ to 64bit) and NCCL ($3.11\times$ to inplace and $3.00\times$ to out-of-place). For 2 nodes, we achieve $1.31\times$ bandwidth improvement to NVSHMEM-64bit and $1.38\times$ to NVSHMEM-32bit.

Low-latency AllToAll

For expert-parallel MoE, AllToAll is mainly used for tokens communication among experts. Previous work such as DeepEP [36] implements extremely high-performance AllToAll kernels for both training and inference. Although providing high performance, the implementation takes thousands lines of CUDA code and is extremely hard to maintain. To demonstrate the advantage of our compiler, we re-implement the AllToAll kernel for inference with only hundreds lines of Python code. We test the inference kernel and scale the number of GPUs from 8 to 64. The results are shown in Figure 16. Our Python kernel consistently exceeds

Table 5 Test Shapes for MoE ReduceScatter and Performance (ms).

Name	tokens/rank	in hidden	out hidden	experts	topk	Ours		PyTorch	
						Intra	Inter	Intra	Inter
MoE-RS-1	1024	1536	2048	8	2	0.51	3.62	4.35	12.41
MoE-RS-2	1024	1536	2048	32	2	0.55	3.90	13.89	33.05
MoE-RS-3	1024	1536	2048	64	2	0.67	4.82	27.91	61.70
MoE-RS-4	1024	1536	2048	32	5	0.92	7.78	14.48	35.35
MoE-RS-5	1024	1536	2048	64	5	0.93	8.25	29.96	64.88
MoE-RS-6	1024	2048	4096	8	2	0.98	7.00	5.02	17.93
MoE-RS-7	1024	2048	4096	32	2	1.08	7.86	14.12	38.24
MoE-RS-8	1024	2048	4096	64	2	1.34	9.87	28.61	66.48
MoE-RS-9	1024	2048	4096	32	5	1.84	15.51	16.70	44.37
MoE-RS-10	1024	2048	4096	64	5	1.86	16.60	27.71	71.82

DeepEP except for AllToAll Dispatch on 64 GPUs. The average speedup of AllToAll Dispatch is $1.18\times$, while the speedup of AllToAll Combine is $1.44\times$. Note that although we implement the same functionality as DeepEP, some details are different. First of all, we use IBRC, while DeepEP uses IBGDA. For intra-node communication, we use NVLink, while DeepEP only uses IB. DeepEP implements a much more complicated logic to control memory queue, which is aimed to reduce the waste of GPU memory. But the memory management logic incurs additional overhead. However, we allocate a much larger memory buffer than DeepEP and omit the memory control logic. As a result, we can achieve better performance compared to DeepEP. We also test larger GPU clusters (e.g. 128 GPUs), the results show that DeepEP still produces the best performance. The reason behind this is that DeepEP uses IBGDA, which has better scalability than IBRC. To further improve our performance, we need to use IBGDA to re-implement our kernel. However, current NVSHMEM bitcode library doesn't support IBGDA. So we leave this for future work.

4.3 Intra-node Kernel Performance on AMD GPUs

To demonstrate the generality of our compiler, we also show the performance on AMD GPUs. We use MI308X GPUs within one node and use AG+GEMM and GEMM+RS to show the performance. The results are shown in Figure 17 and Figure 18. Our baseline is AMD PyTorch+RCCL (PyTorch uses rocBLAS, and rocBLAS provides state-of-the-art GEMM kernels on AMD GPUs). The performance of the code generated by Triton is slightly lower than that of rocBLAS. Even so, we manage to achieve better overlapping performance. For AG+GEMM, we achieve an average speedup of $1.09\times$. For GEMM+RS, we achieve an average speedup of $1.16\times$.

5 Conclusion

Distributed programming and accelerator code development have long been challenging problems for many AI infrastructure developers. In the past, the approach relying on low-level programming led to an excessively development difficulty, and the resulting code was extremely difficult to maintain. To address this issue, we propose Triton-distributed. By integrating distributed capabilities into the Triton compiler, we unify the programming languages for distributed kernels and computational kernels. The required development can be completed at the Python level, and in various operators verification experiments, we have demonstrate that the code generation results of our approach can rival hand-written code. This work is fundamental, providing the underlying infrastructure for more developers to engage in distributed development in the future. Our method can be migrated to multiple types of chips.

References

- [1] AMD. Rocm communication collectives library. <https://github.com/ROCm/rccl>, 2024.
- [2] Cambricon. Triton-linalg for mlu, 2024. URL <https://github.com/Cambricon/triton-linalg>.
- [3] Li-Wen Chang, Wenlei Bao, Qi Hou, Chengquan Jiang, Ningxin Zheng, Yinmin Zhong, Xuanrun Zhang, Zuquan Song, Ziheng Jiang, Haibin Lin, Xin Jin, and Xin Liu. FLUX: fast software-based communication overlap on gpus through kernel fusion. *CoRR*, abs/2406.06858, 2024. doi: 10.48550/ARXIV.2406.06858. URL <https://doi.org/10.48550/arXiv.2406.06858>.
- [4] Chang Chen, Xiuhong Li, Qianchao Zhu, Jiangfei Duan, Peng Sun, Xingcheng Zhang, and Chao Yang. Centauri: Enabling efficient scheduling for communication-computation overlap in large model training via communication partitioning. In Rajiv Gupta, Nael B. Abu-Ghazaleh, Madan Musuvathi, and Dan Tsafir, editors, *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*, Volume 3, ASPLOS 2024, La Jolla, CA, USA, 27 April 2024– 1 May 2024, pages 178–191. ACM, 2024. doi: 10.1145/3620666.3651379. URL <https://doi.org/10.1145/3620666.3651379>.
- [5] Tianqi Chen, Thierry Moreau, Ziheng Jiang, Lianmin Zheng, Eddie Q. Yan, Haichen Shen, Meghan Cowan, Leyuan Wang, Yuwei Hu, Luis Ceze, Carlos Guestrin, and Arvind Krishnamurthy. TVM: an automated end-to-end optimizing compiler for deep learning. In Andrea C. Arpaci-Dusseau and Geoff Voelker, editors, *13th USENIX Symposium on Operating Systems Design and Implementation, OSDI 2018, Carlsbad, CA, USA, October 8-10, 2018*, pages 578–594. USENIX Association, 2018.
- [6] Tri Dao, Daniel Haziza, Francisco Massa, and Grigory Sizov. Flash-decoding for long-context inference, 2023. URL <https://crfm.stanford.edu/2023/10/12/flashdecoding.html>.
- [7] DeepSeek-AI, Aixin Liu, Bei Feng, Bing Xue, Bingxuan Wang, Bochao Wu, Chengda Lu, Chenggang Zhao, Chengqi Deng, Chenyu Zhang, Chong Ruan, Damai Dai, Daya Guo, Dejian Yang, Deli Chen, Dongjie Ji, Erhang Li, Fangyun Lin, Fucong Dai, Fuli Luo, Guangbo Hao, Guanting Chen, Guowei Li, H. Zhang, Han Bao, Hanwei Xu, Haocheng Wang, Haowei Zhang, Honghui Ding, Huajian Xin, Huazuo Gao, Hui Li, Hui Qu, J. L. Cai, Jian Liang, Jianzhong Guo, Jiaqi Ni, Jiashi Li, Jiawei Wang, Jin Chen, Jingchang Chen, Jingyang Yuan, Junjie Qiu, Junlong Li, Junxiao Song, Kai Dong, Kai Hu, Kaige Gao, Kang Guan, Kexin Huang, Kuai Yu, Lean Wang, Lecong Zhang, Lei Xu, Leyi Xia, Liang Zhao, Litong Wang, Liyue Zhang, Meng Li, Miaoju Wang, Mingchuan Zhang, Minghua Zhang, Minghui Tang, Mingming Li, Ning Tian, Panpan Huang, Peiyi Wang, Peng Zhang, Qiancheng Wang, Qihao Zhu, Qinyu Chen, Qiushi Du, R. J. Chen, R. L. Jin, Ruiqi Ge, Ruisong Zhang, Ruizhe Pan, Runji Wang, Runxin Xu, Ruoyu Zhang, Ruyi Chen, S. S. Li, Shanghao Lu, Shangyan Zhou, Shanhuang Chen, Shaoqing Wu, Shengfeng Ye, Shengfeng Ye, Shirong Ma, Shiyu Wang, Shuang Zhou, Shuiping Yu, Shunfeng Zhou, Shuting Pan, T. Wang, Tao Yun, Tian Pei, Tianyu Sun, W. L. Xiao, and Wangding Zeng. Deepseek-v3 technical report. *CoRR*, abs/2412.19437, 2024. doi: 10.48550/ARXIV.2412.19437. URL <https://doi.org/10.48550/arXiv.2412.19437>.
- [8] Tyler Denniston, Shoaib Kamil, and Saman P. Amarasinghe. Distributed halide. In Rafael Asenjo and Tim Harris, editors, *Proceedings of the 21st ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPOPP 2016, Barcelona, Spain, March 12-16, 2016*, pages 5:1–5:12. ACM, 2016. doi: 10.1145/2851141.2851157. URL <https://doi.org/10.1145/2851141.2851157>.
- [9] Siyuan Feng, Bohan Hou, Hongyi Jin, Wuwei Lin, Junru Shao, Ruihang Lai, Zihao Ye, Lianmin Zheng, Cody Hao Yu, Yong Yu, and Tianqi Chen. Tensorir: An abstraction for automatic tensorized program optimization. In Tor M. Aamodt, Natalie D. Enright Jerger, and Michael M. Swift, editors, *Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2, ASPLOS 2023, Vancouver, BC, Canada, March 25-29, 2023*, pages 804–817. ACM, 2023. doi: 10.1145/3575693.3576933. URL <https://doi.org/10.1145/3575693.3576933>.
- [10] Google. Pallas, 2025. URL <https://docs.jax.dev/en/latest/pallas/index.html>.
- [11] Georgios I. Goumas, Aristidis Sotiropoulos, and Nectarios Koziris. Minimizing completion time for loop tiling with computation and communication overlapping. In *Proceedings of the 15th International Parallel & Distributed Processing Symposium (IPDPS-01)*, San Francisco, CA, USA, April 23-27, 2001, page 39. IEEE Computer Society, 2001. doi: 10.1109/IPDPS.2001.924976. URL <https://doi.org/10.1109/IPDPS.2001.924976>.
- [12] Yanping Huang, Youlong Cheng, Ankur Bapna, Orhan Firat, Dehao Chen, Mia Xu Chen, HyoukJoong Lee, Jiquan Ngiam, Quoc V. Le, Yonghui Wu, and Zhifeng Chen. Gpipe: Efficient training of giant neural networks using pipeline parallelism. In Hanna M. Wallach, Hugo Larochelle, Alina Beygelzimer, Flo-

- rence d’Alché-Buc, Emily B. Fox, and Roman Garnett, editors, *Advances in Neural Information Processing Systems 32: Annual Conference on Neural Information Processing Systems 2019, NeurIPS 2019, December 8-14, 2019, Vancouver, BC, Canada*, pages 103–112, 2019. URL <https://proceedings.neurips.cc/paper/2019/hash/093f65e080a295f8076b1c5722a46aa2-Abstract.html>.
- [13] Zhihao Jia, Oded Padon, James J. Thomas, Todd Warszawski, Matei Zaharia, and Alex Aiken. TASO: optimizing deep learning computation with automatic generation of graph substitutions. In Tim Brecht and Carey Williamson, editors, *Proceedings of the 27th ACM Symposium on Operating Systems Principles, SOSP 2019, Huntsville, ON, Canada, October 27-30, 2019*, pages 47–62. ACM, 2019. doi: 10.1145/3341301.3359630. URL <https://doi.org/10.1145/3341301.3359630>.
 - [14] Fredrik Kjolstad, Shoaib Kamil, Stephen Chou, David Lugato, and Saman P. Amarasinghe. The tensor algebra compiler. *Proc. ACM Program. Lang.*, 1(OOPSLA):77:1–77:29, 2017. doi: 10.1145/3133901. URL <https://doi.org/10.1145/3133901>.
 - [15] Chris Lattner, Jacques A. Pienaar, Mehdi Amini, Uday Bondhugula, River Riddle, Albert Cohen, Tatiana Shpeisman, Andy Davis, Nicolas Vasilache, and Oleksandr Zinenko. MLIR: A compiler infrastructure for the end of moore’s law. *CoRR*, abs/2002.11054, 2020. URL <https://arxiv.org/abs/2002.11054>.
 - [16] Huiwei Lu, Sangmin Seo, and Pavan Balaji. MPI+ULT: overlapping communication and computation with user-level threads. In *17th IEEE International Conference on High Performance Computing and Communications, HPCC 2015, 7th IEEE International Symposium on Cyberspace Safety and Security, CSS 2015, and 12th IEEE International Conference on Embedded Software and Systems, ICESS 2015, New York, NY, USA, August 24-26, 2015*, pages 444–454. IEEE, 2015. doi: 10.1109/HPCC-CSS-ICISS.2015.82. URL <https://doi.org/10.1109/HPCC-CSS-ICISS.2015.82>.
 - [17] Vladimir Marjanovic, Jesús Labarta, Eduard Ayguadé, and Mateo Valero. Overlapping communication and computation by using a hybrid mpi/smpss approach. In Taisuke Boku, Hiroshi Nakashima, and Avi Mendelson, editors, *Proceedings of the 24th International Conference on Supercomputing, 2010, Tsukuba, Ibaraki, Japan, June 2-4, 2010*, pages 5–16. ACM, 2010. doi: 10.1145/1810085.1810091. URL <https://doi.org/10.1145/1810085.1810091>.
 - [18] Deepak Narayanan, Mohammad Shoeybi, Jared Casper, Patrick LeGresley, Mostofa Patwary, Vijay Korthikanti, Dmitri Vainbrand, Prethvi Kashinkunti, Julie Bernauer, Bryan Catanzaro, Amar Phanishayee, and Matei Zaharia. Efficient large-scale language model training on GPU clusters using megatron-lm. In Bronis R. de Supinski, Mary W. Hall, and Todd Gamblin, editors, *International Conference for High Performance Computing, Networking, Storage and Analysis, SC 2021, St. Louis, Missouri, USA, November 14-19, 2021*, page 58. ACM, 2021. doi: 10.1145/3458817.3476209. URL <https://doi.org/10.1145/3458817.3476209>.
 - [19] NVIDIA. cuBLAS, 2022. URL <https://developer.nvidia.com/cublas>.
 - [20] Nvidia. Cutlass, 2022. URL <https://github.com/NVIDIA/cutlass>.
 - [21] NVIDIA. Nvidia collective communications library. <https://developer.nvidia.com/nccl>, 2024.
 - [22] OpenAI. Chatgpt, 2022. URL <https://chat.openai.com/>.
 - [23] OpenAI. Sora, 2024. URL <https://openai.com/sora/>.
 - [24] OpenAI. Addendum to gpt-4o system card: Native image generation. 2025. URL https://cdn.openai.com/11998be9-5319-4302-bfbf-1167e093f1fb/Native_Image_Generation_System_Card.pdf.
 - [25] Kishore Punniyamurthy, Khaled Hamidouche, and Bradford M Beckmann. Optimizing distributed ml communication with fused computation-collective operations. *arXiv preprint arXiv:2305.06942*, 2023.
 - [26] Jonathan Ragan-Kelley, Connelly Barnes, Andrew Adams, Sylvain Paris, Frédo Durand, and Saman P. Amarasinghe. Halide: a language and compiler for optimizing parallelism, locality, and recomputation in image processing pipelines. In *ACM SIGPLAN Conference on Programming Language Design and Implementation, PLDI ’13, Seattle, WA, USA, June 16-19, 2013*, pages 519–530, 2013. doi: 10.1145/2491956.2462176. URL <https://doi.org/10.1145/2491956.2462176>.
 - [27] Jeff Rasley, Samyam Rajbhandari, Olatunji Ruwase, and Yuxiong He. Deepspeed: System optimizations enable training deep learning models with over 100 billion parameters. In Rajesh Gupta, Yan Liu, Jiliang Tang, and B. Aditya Prakash, editors, *KDD ’20: The 26th ACM SIGKDD Conference on Knowledge Discovery and Data*

- Mining, Virtual Event, CA, USA, August 23-27, 2020, pages 3505–3506. ACM, 2020. doi: 10.1145/3394486.3406703. URL <https://doi.org/10.1145/3394486.3406703>.
- [28] ByteDance Seed. Doubao-1.5-pro, 2025. URL https://team.doubao.com/en/special/doubao_1_5_pro.
- [29] Hari Subramoni, Sourav Chakraborty, and Dhabaleswar K. Panda. Designing dynamic and adaptive MPI point-to-point communication protocols for efficient overlap of computation and communication. In Julian M. Kunkel, Rio Yokota, Pavan Balaji, and David E. Keyes, editors, *High Performance Computing - 32nd International Conference, ISC High Performance 2017, Frankfurt, Germany, June 18-22, 2017, Proceedings*, volume 10266 of *Lecture Notes in Computer Science*, pages 334–354. Springer, 2017. doi: 10.1007/978-3-319-58667-0_18. URL https://doi.org/10.1007/978-3-319-58667-0_18.
- [30] Qwen Team. Qwen2.5 technical report. *arXiv preprint arXiv:2412.15115*, 2024.
- [31] TileLang Team. Tilelang, 2025. URL <https://github.com/tile-ai/tilelang>.
- [32] Philippe Tillet, Hsiang-Tsung Kung, and David D. Cox. Triton: an intermediate language and compiler for tiled neural network computations. In Tim Mattson, Abdullah Muzahid, and Armando Solar-Lezama, editors, *Proceedings of the 3rd ACM SIGPLAN International Workshop on Machine Learning and Programming Languages, MAPL@PLDI 2019, Phoenix, AZ, USA, June 22, 2019*, pages 10–19. ACM, 2019. doi: 10.1145/3315508.3329973. URL <https://doi.org/10.1145/3315508.3329973>.
- [33] Rohan Yadav, Alex Aiken, and Fredrik Kjolstad. DISTAL: the distributed tensor algebra compiler. In Ranjit Jhala and Isil Dillig, editors, *PLDI '22: 43rd ACM SIGPLAN International Conference on Programming Language Design and Implementation, San Diego, CA, USA, June 13 - 17, 2022*, pages 286–300. ACM, 2022. doi: 10.1145/3519939.3523437. URL <https://doi.org/10.1145/3519939.3523437>.
- [34] Zihao Ye, Lequn Chen, Ruihang Lai, Wuwei Lin, Yineng Zhang, Stephanie Wang, Tianqi Chen, Baris Kasikci, Vinod Grover, Arvind Krishnamurthy, and Luis Ceze. Flashinfer: Efficient and customizable attention engine for llm inference serving. *arXiv preprint arXiv:2501.01005*, 2025. URL <https://arxiv.org/abs/2501.01005>.
- [35] Shulai Zhang, Ningxin Zheng, Haibin Lin, Ziheng Jiang, Wenlei Bao, Chengquan Jiang, Qi Hou, Weihao Cui, Size Zheng, Li-Wen Chang, Quan Chen, and Xin Liu. Comet: Fine-grained computation-communication overlapping for mixture-of-experts. *CoRR*, abs/2502.19811, 2025. doi: 10.48550/ARXIV.2502.19811. URL <https://doi.org/10.48550/arXiv.2502.19811>.
- [36] Chenggang Zhao, Shangyan Zhou, Liyue Zhang, Chengqi Deng, Zhean Xu, Yuxuan Liu, Kuai Yu, Jiashi Li, and Liang Zhao. DeepEP: an efficient expert-parallel communication library. <https://github.com/deepseek-ai/DeepEP>, 2025.
- [37] Lianmin Zheng, Chengfan Jia, Minmin Sun, Zhao Wu, Cody Hao Yu, Ameer Haj-Ali, Yida Wang, Jun Yang, Danyang Zhuo, Koushik Sen, Joseph E. Gonzalez, and Ion Stoica. Ansor: Generating high-performance tensor programs for deep learning. In *14th USENIX Symposium on Operating Systems Design and Implementation, OSDI 2020, Virtual Event, November 4-6, 2020*, pages 863–879. USENIX Association, 2020. URL <https://www.usenix.org/conference/osdi20/presentation/zheng>.
- [38] Size Zheng, Yun Liang, Shuo Wang, Renze Chen, and Kaiwen Sheng. FlexTensor: An automatic schedule exploration and optimization framework for tensor computation on heterogeneous system. In James R. Larus, Luis Ceze, and Karin Strauss, editors, *ASPLOS '20: Architectural Support for Programming Languages and Operating Systems, Lausanne, Switzerland, March 16-20, 2020 [ASPLOS 2020 was canceled because of COVID-19]*, pages 859–873. ACM, 2020. doi: 10.1145/3373376.3378508. URL <https://doi.org/10.1145/3373376.3378508>.
- [39] Size Zheng, Renze Chen, Anjiang Wei, Yicheng Jin, Qin Han, Liqiang Lu, Bingyang Wu, Xiuhong Li, Shengen Yan, and Yun Liang. AMOS: enabling automatic mapping for tensor computations on spatial accelerators with hardware abstraction. In Valentina Salapura, Mohamed Zahran, Fred Chong, and Lingjia Tang, editors, *ISCA '22: The 49th Annual International Symposium on Computer Architecture, New York, New York, USA, June 18 - 22, 2022*, pages 874–887. ACM, 2022. doi: 10.1145/3470496.3527440. URL <https://doi.org/10.1145/3470496.3527440>.
- [40] Size Zheng, Jin Fang, Xuegui Zheng, Qi Hou, Wenlei Bao, Ningxin Zheng, Ziheng Jiang, Dongyang Wang, Jianxi Ye, Haibin Lin, Li-Wen Chang, and Xin Liu. Tilelink: Generating efficient compute-communication overlapping kernels using tile-centric primitives, 2025. URL <https://arxiv.org/abs/2503.20313>.